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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/810,033	03/26/2004	Jean-Michel Daga	ATM-276	8427

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EXAMINER	
TRA, ANH QUAN	

ART UNIT	PAPER NUMBER
2816	

DATE MAILED: 06/17/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/810,033	DAGA ET AL.	
	Examiner	Art Unit	
	Quan Tra	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 March 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-18* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 6/21/04; 6/24/04; 8/30/04; 12/27/04
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claim 9 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 9 is indefinite because there is no antecedent basis for the limitation "each of said structure".

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claims 1-6, 10-12 are rejected under 35 U.S.C. 102(b) as being anticipated by Kim et al. (US 20020122324).

As to claim 1, Kim et al. discloses in figure 5 an apparatus for generating a supply voltage internally within an integrated circuit comprising: a charge pump stage structure having a pumping capacitor (CP2) connected to a pumping node (node between PT1 and PT2), a first

PMOS device (PT1) connected to an input node, the first PMOS device configured to electrically communicate with the pumping capacitor, wherein the first PMOS device is configured to connect the pumping node to the input node when the pumping capacitor is not boosted; a second PMOS device (PT2) connected to an output node, the second PMOS device configured to electrically communicate with the pumping capacitor, the second PMOS device configured to transfer electrical charge from the pumping node to the output node when the pumping capacitor is boosted, the second PMOS device configured to prevent a reversal current feedback from the output node to the pumping node when the pumping capacitor is not boosted; and a third PMOS device (MPB1) configured to electrically communicate with the first PMOS device, wherein the third PMOS device is configured to connect the pumping node to a gate of the second PMOS device to prevent the current feedback.

As to claim 2, figure 5 shows that the third PMOS device is configured to connect the pump node to a gate of the second device in order to prevent the current feedback from the pumping node to the input node when the pumping capacitor is boosted.

As to claim 3, figure 5 shows an auxiliary capacitor (CB1) connected to the first PMOS device, wherein the auxiliary capacitor is configured to generate an undershoot on the gate of the first PMOS device, and wherein the auxiliary capacitor is configured to switch the apparatus to an "ON" state when an electrical current is transferred from the input node to the pumping node.

As to claims 4-6 and 10-12, figure 8 shows a symmetrical charge pump having first independent structure (the upper circuit) and second independent structure (the lower circuit), wherein each independent structure has similar configuration as circuit figure 5.

Claim 7 recites similar limitations of claims 1-3. Therefore, they are rejected for the same reasons.

As to claim 8, figure 5 shows the third PMOS device is configured to switch a gate of the first PMOS device to a boosted pump node potential in order to prevent the current feedback from the pumping node to the input control node when the pumping capacitor is boosted.

Insofar as understood to claim 9, figure 5 shows an auxiliary capacitor (CB1) connected to the first PMOS device, wherein the auxiliary capacitor is configured to generate an undershoot on the gate of the first PMOS device, and wherein the auxiliary capacitor is configured to switch the apparatus to an "ON" state when an electrical current is transferred from the input control node to said pumping node.

5. Claims 1, 2, 4, 5, 10 and 11 are rejected under 35 U.S.C. 102(e) as being anticipated by Yen (US 2004/0104761).

As to claim 1, Yen discloses in figure 5 an apparatus for generating a supply voltage internally within an integrated circuit comprising: a charge pump stage structure having a pumping capacitor (540) connected to a pumping node (552), a first PMOS device (506) connected to an input node (VIN), the first PMOS device configured to electrically communicate with the pumping capacitor, wherein the first PMOS device is configured to connect the pumping node to the input node when the pumping capacitor is not boosted; a second PMOS device (566) connected to an output node (590), the second PMOS device configured to electrically communicate with the pumping capacitor, the second PMOS device configured to transfer electrical charge from the pumping node to the output node when the pumping capacitor is boosted, the second PMOS device configured to prevent a reversal current feedback from the

output node to the pumping node when the pumping capacitor is not boosted; and a third PMOS device (508) configured to electrically communicate with the first PMOS device, wherein the third PMOS device is configured to connect the pumping node to a gate of the second PMOS device to prevent the current feedback.

As to claim 2, figure 5 shows that the third PMOS device is configured to connect the pump node to a gate of the second device in order to prevent the current feedback from the pumping node to the input node when the pumping capacitor is boosted.

As to claims 4, 5 and 10, figure 5 is a symmetrical charge pump.

As to claim 11, figure 5 shows that third PMOS device is configured to switch a gate of the first PMOS device to a boosted pump node potential in order to prevent the current feedback from the pumping node to the input control node when the pumping capacitor is boosted.

6. Claims 13, 14, 16 and 17 are rejected under 35 U.S.C. 102(e) as being anticipated by Min (USP 6734717).

As to claim 13, Min's figure 2 shows an apparatus for generating a supply voltage internally within an integrated circuit comprising: a plurality symmetrical charge pump stages (PS1-PS3) cascade-connected in series having: a first symmetrical pump charge stage (PS1) connected to an input node; and a last symmetrical pump charge stage (PS3) connected to an output node.

As to claim 14, figure 2 shows at least one intermediate symmetrical pump charge stage (PS2) therebetween.

Claims 16 and 17 recite similar limitations of claims 13 and 14. Therefore, they are rejected for the same reasons.

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claims 15 and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yen (US 2004/0104761) in view of Min (USP 6734717).

Yen's figure 5 shows all limitations of the claims except for plurality of charge pump stages connected in series. However, Min's figure 2 shows a charge pump circuit having plurality of charge pump stages connected in series in order to increase the output voltage. Therefore, it would have been obvious to one having ordinary skill in the art to add plurality of charge pump stages connected in series to Yen's charge pump stage for the purpose of increasing the output voltage level.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Quan Tra whose telephone number is 571-272-1755. The examiner can normally be reached on 8:00 A.M.-5:00 P.M..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Callahan can be reached on 571-272-1740. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Quan Tra
Primary Examiner

June 15, 2005